A New Extraction Method to Determine Bias-Dependent Source Series Resistance in GaAs FET's

Chung-Hwan Kim, Kyung-Sik Yoon, *Member, IEEE,* Jeon-Wook Yang, Jin-Hee Lee, Chul-Soon Park, *Member, IEEE,* Jae-Jin Lee, and Kwang-Eui Pyun, *Member, IEEE*

***Abstract*— A new method is proposed to determine bias-dependent source resistances for GaAs field-effect transistors (FET's). This method, which is a cold-FET measurement technique, utilizes the relations between the real part of the two-port impedances transformed from the measured S-parameters and their algebraic derivatives. It is based on the fact that the algebraic derivatives of the two-port resistances result in the simple form at the normal cold-FET condition. A bias-independent gate resistance is extracted at the pinched-off cold-FET condition to fulfill necessary and sufficient conditions in extraction. The proposed method is a direct measurement because only algebraic calculation is required, and it is general enough to need only one assumption of the laterally symmetric channel-doping profile. The deleterious results of dispersion (frequency dependence) and negative value in source resistances at the pinched-off cold-FET condition are explained by the effects of the leakage current and the on-wafer pad parasitics, respectively. The problem of deviation of α_{21} and α_{12} from 0.5 at the normal cold-FET condition is also resolved by deembedding the on-wafer pad parasitics. This method allows one to extract bias-dependent source resistances for GaAs FET's.**

***Index Terms*—Bias dependence, cold FET, source resistance.**

I. Introduction

ACCURATE modeling, characterization, and optimization of GaAs field-effect transistors (FET's) are very important for the development of GaAs device technology. In modeling FET's using lumped-element equivalent circuits, numerical optimization techniques have problems of uniqueness and long execution times. Numerical techniques to improve and/or solve the problems have been proposed [1], [2]. However, they require at least somewhat cumbersome iterations. Therefore, determination of the extrinsic parameters such as parasitic resistances and reactances before modeling the intrinsic part is considered essential to solve these problems [3]. As the GaAs device technology advances, FET's with submicrometer gate length have been popular. For FET's with submicrometer gate length, the parasitic resistances can limit the performance of FET's. Although source and drain resistances have been regarded as bias independent, the validity of the assumption must be examined carefully. Therefore, the method to determine bias-dependent parasitic resistances is needed. Although several techniques to obtain parasitic resistances have been proposed, most of the previous techniques have been based on the assumption that source and drain resistances are gate- and drain-bias independent.

The dc measurement techniques including the so-called end-resistance and gate–probe measurements have been widely used because of their simple and direct measurements [4]–[10]. Since most of the dc measurement techniques are based on the well-known diode current equation, they can measure the parasitic resistances only at the gate conduction region, i.e., forwardly biased gate region. Some authors [9], [10] have reported dc measurement techniques to determine bias-dependent source and drain resistances. Their methods, however, are not practical because they need various FET's with different gate lengths while keeping all the other parameters not changed. The ac techniques of measuring scattering parameters have a potential advantage over dc ones since S-parameters can be measured at all the gate bias ranges [3], [11]–[14]. Among the ac techniques, the normal cold-FET technique (for $V_{\rm ds} = 0$ V and $V_{\rm gs} > V_t$) [3], [11]–[13] is most popular. The previous cold-FET techniques, however, lack how to determine bias-dependent parasitic resistances because the relations between measurements and parasitic resistances should be obtained at finite gate-bias points and/or at the special bias point. The pinched-off cold-FET technique (for $V_{\rm ds} = 0$ V and $V_{\rm gs} < V_t$) [14] is the simplest one, but it has some drawbacks of negative and frequency-dependent source resistance, especially for FET's with narrow gatewidth. In addition, the parasitic resistances can be determined only at the pinched-off bias region. Sommer [15] has proposed a technique to determine bias-dependent source resistance of FET's under active-bias condition. Sommer's method is to determine bias-dependent parasitic resistances from the relation between parasitic resistances and feedback admittance. It is, however, somewhat cumbersome to perform a partial optimization procedure.

In this paper, a new method to determine bias-dependent source resistance is introduced. The method has its origin in the cold-FET measurement technique and is based on the real part of the two-port impedances and their algebraic derivatives. The usefulness of this method is demonstrated by characterizing MESFET's and high electron-mobility transistors (HEMT's) of low-power applications.

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C.-H. Kim, J.-W. Yang, J.-H. Lee, C.-S. Park, J.-J. Lee, and K.-E. Pyun are with the Semiconductor Division, Electronics and Telecommunications Research Institute, Yusong, Taejon 305-600, Korea.

K.-S. Yoon is with the Department of Electronics and Information Engineering, Korea University, Chochiwon, Choon-Nam 339-700, Korea.

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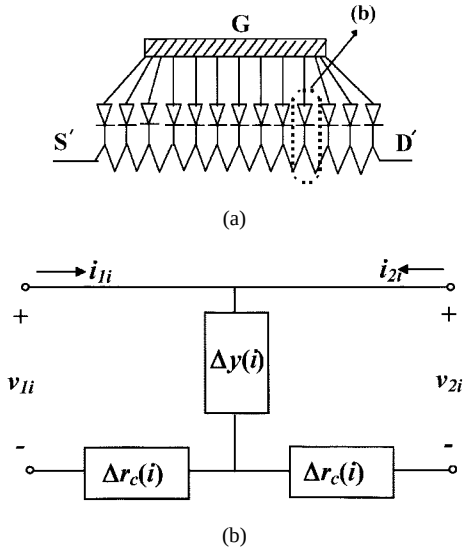


Fig. 1. (a) A model of distributed diodes and channel resistors of the intrinsic part of an FET. (b) An $ABCD$ matrix network of a part of distributed diodes and channel resistors from model.

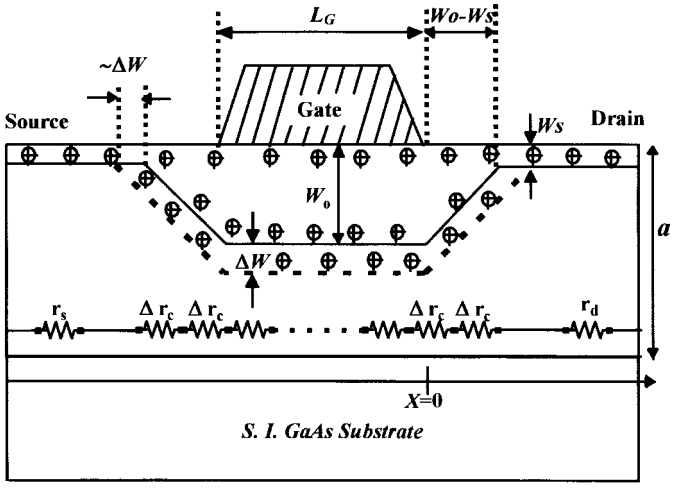


Fig. 2. Laterally symmetric depletion profile is satisfied at the cold-FET condition. The symmetry is preserved when a small change in gate bias occurs. The dotted line represents the changed depletion region by a small gate bias change. The linear depletion approximation out of the gate is adopted for simplicity in calculation.

II. Modeling at the Normally Biased Cold-FET Condition

For an FET biased in the linear region, the intrinsic part can be described as distributed diodes and channel resistors, as shown in Fig. 1(a). An infinitesimal portion of the intrinsic FET as a two-port network is shown in Fig. 1(b). A gate diode and channel resistor of this portion are represented as an admittance and resistance, respectively. Since the infinitesimal FET's should be cascaded, the expression by an $ABCD$ matrix is chosen to obtain two-port current-voltage relations. As derived in Appendix A, the real part of the ac common-source impedance at the normal cold-FET condition can be expressed as

$$\mathrm{re}[z_{11}] = r_g + r_s + \alpha_{11} \cdot r_{\mathrm{ds}} \tag{1}$$

$$\mathrm{re}[z_{21,12}] = r_s + \alpha_{21,12} \cdot r_{\mathrm{ds}} \tag{2}$$

$$\mathrm{re}[z_{22}] = r_s + r_d + r_{\mathrm{ds}} \tag{3}$$

where $\alpha_{21} = \alpha_{12} = 0.5$. For a small change in the gate voltage, all the resistances except r_g should be considered as variables. Under the cold-FET condition, as shown in Fig. 2, the lateral symmetry in the channel-doping profile is preserved even though gate bias is changed. As gate voltage is changed, the change in the common-source FET resistances are expressed as

$$\Delta\mathrm{re}[z_{11}] = \Delta r_s + \Delta\alpha_{11} \cdot r_{\mathrm{ds}} + \alpha_{11} \cdot \Delta r_{\mathrm{ds}} \tag{4a}$$

$$\Delta\mathrm{re}[z_{21}] = \Delta\mathrm{re}[z_{12}] = \Delta r_s + \tfrac{1}{2}\,\Delta r_{\mathrm{ds}} \tag{4b}$$

$$\Delta\mathrm{re}[z_{22}] = \Delta r_s + \Delta r_d + \Delta r_{\mathrm{ds}} = 2 \cdot \Delta r_s + \Delta r_{\mathrm{ds}}. \tag{4c}$$

Here, (4c) is obtained from the condition of the laterally symmetric channel-doping profile, i.e., $\Delta r_s = \Delta r_d$. Since summing $\Delta\mathrm{re}[z_{21}]$ and $\Delta\mathrm{re}[z_{12}]$ in (4b) results in (4c), this equality can be used as a check point of the validity of the assumption. As described in Appendix B, using the linear depletion approximation, as shown in Fig. 2, the changes in the channel and source resistances by gate bias change are approximated as

$$\begin{aligned} |\Delta r_{\mathrm{ds}}| &\approx \rho \cdot |\Delta W|/(a - W_o)^2 \cdot L_G + 2\rho \cdot \frac{|\Delta W|}{a - W_o} \\ &\quad \cdot \tan^{-1}\left(\frac{W_o - W_s}{a - W_o}\right) \\ &\approx (|\Delta W|/(a - W_o)) \cdot r_{\mathrm{ds}} \end{aligned} \tag{5a}$$

and

$$|\Delta r_s| \approx \rho \cdot (|\Delta W|/(a - W_o)) \approx (|\Delta W|/L_{\mathrm{GS}}) \cdot r_s \tag{5b}$$

where W_o is the depletion width under the gate metal, W_s is the surface depletion width, L_G is the gate length, L_{GS} is the gap between gate–edge to source ohmic region, ρ is the resistivity per gatewidth of the channel, a is total channel depth, and ΔW is the change in the depletion width by the change in the dc gate bias. In (5b), the contribution of the ohmic contact to r_s is ignored to simplify the following argument. From (5a) and (5b), Δr_s and Δr_d can be neglected compared to Δr_{ds} under the following condition:

$$((a - W_o)/L_{\mathrm{GS,GD}}) \cdot (r_{s,d}/r_{\mathrm{ds}}) \ll 1. \tag{6}$$

Actually, condition (6) limits the maximum gate voltage where our method is applicable. In [6], the value of a_{11} has been proven to be 1/3 and independent of gate bias change if the lateral channel resistance per gate length is uniform. Therefore, if the nonuniformity in the channel resistance per gate length is not severe, $\Delta\alpha_{11}$ is, at most, proportional to $(\Delta W)^2$. The change in the depletion width ΔW can be made as small as possible by adjusting the dc gate voltage change, thereby, $\Delta\alpha_{11} \cdot r_{\mathrm{ds}}$ can also be neglected within the specified error. When the condition of (6) is satisfied and the change of gate bias is small, α_{11} can be obtained by the following relation:

$$\alpha_{11} \approx \Delta\mathrm{re}[z_{11}]/\Delta\mathrm{re}[z_{22}] \quad \text{or} \quad 2 \cdot \Delta\mathrm{re}[z_{11}]/\Delta\mathrm{re}[z_{21,12}]. \tag{7}$$

Although values of α_{12} and α_{21} are 0.5, as proven in Appendix A, they can be obtained from the measurement by the

TABLE I
SUMMARY OF GEOMETRICAL PARAMETERS, EXTRACTED PARASITIC RESISTANCES AND AVERAGES α_{ij}'s

	MESFET A	MESFET B	HEMT
UGW	100 μm	100 μm	50 μm
no. of fingers	2	2	2
L_G	1.1 μm	0.7 μm	0.15 μm
L_{GS}	0.7 μm	0.6 μm	1.0 μm
L_{GD}	1.3 μm	0.7 μm	1.9 μm
V_p	~ -0.7V	~ -0.5V	~ -0.5V
R_p	0.75 MΩ	0.37 MΩ	0.55 MΩ
r_g	3.2 Ω	4.5 Ω	2.2 Ω
r_s @ V_{GS}=0V	2.7 Ω	2.5 Ω	3.0 Ω
r_d @ V_{GS}=0V	6.0 Ω	3.8 Ω	6.4 Ω
$<\alpha_{11}>$	0.310	0.293	0.290
$<\alpha_{21}>$	0.499	0.502	0.505

following equations:

$$\alpha_{21} \sim \Delta\mathrm{re}[z_{21}]/\Delta\mathrm{re}[r_{22}] \tag{8}$$

and

$$\alpha_{12} \approx \Delta\mathrm{re}[z_{21}]/\Delta\mathrm{re}[z_{22}]. \tag{9}$$

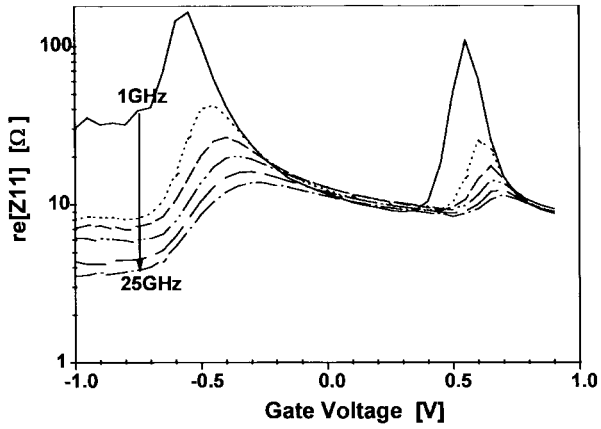
Equations (8) and (9) are valid when condition (6) is satisfied.

To obtain (1)–(3), the laterally symmetric channel-doping profile was only assumed. The drain resistance is generally larger than the source resistance because a smaller source resistance is required to enhance the speed and reduce the noise of the device. Simultaneously, a larger drain resistance is generally adopted to satisfy the breakdown voltage requirement and usually it can be accomplished by increasing the gap between the gate metal and drain ohmic region. The symmetric channel-doping profile is, however, not violated in most cases because the depletion regions out of the gate edge produced by the gate-bias change in the cold-FET condition is narrow enough not to touch the ohmic contact regions. Hence, the symmetric channel profile can be accepted without loss of generality and this gives the same gate bias dependence of r_s and r_d, i.e., $\Delta r_s = \Delta r_d$.

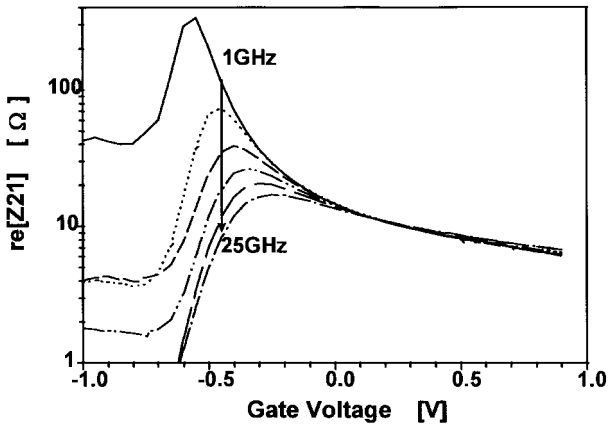
III. MODELING AT THE PINCHED-OFF COLD-FET CONDITION

As shown in Appendix C, the gate resistance can be obtained at the pinched-off cold-FET condition as a fitting parameter of the following relation:

$$\mathrm{re}[z_{11}] - \mathrm{re}[z_{21}] = r_g + R_p \cdot \frac{(2\tau_p + \tau_{\mathrm{ds}}) \cdot \tau_{\mathrm{ds}} \cdot \omega^2}{[1+\tau_p^2\omega^2] \cdot [1+(\tau_p + 2\tau_{\mathrm{ds}})^2\omega^2]} \tag{10}$$



(a)



(b)

Fig. 3. Frequency and bias dependence of measured $\mathrm{re}[z_{ij}]$'s for MESFET B. (a) $\mathrm{re}[z_{11}]$, and (b) $\mathrm{re}[z_{21}]$.

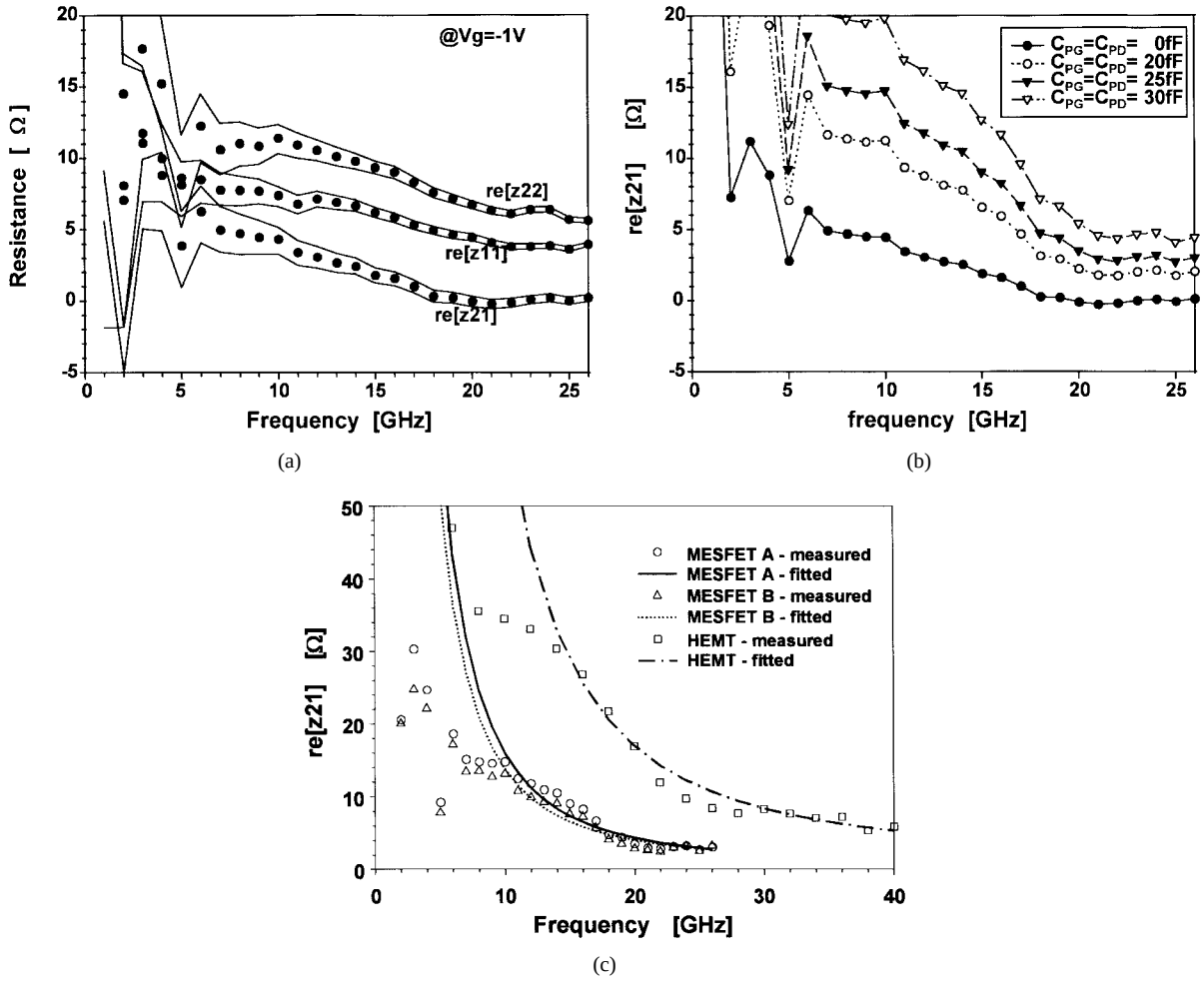


Fig. 4. Frequency dependence of resistances at the pinched-off cold-FET condition. (a) Dispersion of measured $\mathrm{re}[z_{ij}]$'s at $V_{\mathrm{gs}} = -1$ V for MESFET B. Solid lines represent min.–max. bound caused by the VNA calibration error. (b) $\mathrm{re}[z_{21}]$ after deembedding-pad parasitic capacitance at the pinched-off bias condition ($V_{\mathrm{gs}} = -1$ V) for MESFET B. (c) Dispersion fitting of the measured and then pad-deembedded $\mathrm{re}[z_{21}]$'s of three types of FET's.

where $\tau_p = R_p \cdot C_p$ and $\tau_{\mathrm{ds}} = R_p \cdot C_{\mathrm{ds}}$. When the leakage current can be ignored ($R_p \to \infty$) and/or the frequency is high enough ($\omega \to \infty$), (10) is reduced to the original one [14] as $r_g \to \mathrm{re}[z_{11}] - \mathrm{re}[z_{21}]$.

IV. Measurements and Discusssions

Bias-dependent source resistances were determined for two types of MESFET's and an HEMT. They have gate lengths of 1.1, 0.7, and 0.15 μm, respectively. For our convenience, they are named as MESFET A, MESFET B, and HEMT, respectively. The detailed processes and characteristics of FET's have been published elsewhere [16], [17]. Other parameters are summarized in Table I. Scattering parameters of the FET's were measured by HP8510B and HP8510C vector network analyzers (VNA's) for the frequencies up to 40 GHz. DC bias was supplied by an HP4142B. The VNA calibration was done by short-open-load-thru (SOLT). Fig. 3 shows the real part of the z-parameters transformed from the measured scattering parameters at the cold-FET condition for MESFET B. Although not shown, the frequency dependence of $\mathrm{re}[z_{22}]$ and $\mathrm{re}[z_{12}]$ is nearly similar to that of $\mathrm{re}[z_{21}]$ in Fig. 3(b). From the bias and frequency dependence of the real part of the z-parameters, the following phenomena were observed:

1) peak of $\mathrm{re}[z_{11}]$ near the turn-on gate voltage;
2) peaks near pinched-off bias are observed for all the $\mathrm{re}[z_{ij}]$'s;
3) $\mathrm{re}[z_{21}]$ transformed from the measured scattering parameters at the pinched-off bias shows appreciable frequency dependence and negative value at high-frequency range.

Firstly, the peaks of $\mathrm{re}[z_{11}]$ near the turn-on gate voltage are known to be caused by the distributed capacitors and small-valued resistors of the gate diode [3], [11]. Concerning 2), although not explicitly explained in the other works for the peaks near pinched-off bias, these are caused by the distributed diodes and large-valued channel resistors. The peaks near the pinched-off bias could be realized in the circuit simulator using a finite number of diodes and resistors. Concerning 3), frequency-dependent and negative source resistance from the measured and then transformed scattering parameters is also shown in Fig. 4(a) and (b). The dispersion at the pinched cold-FET is also shown for the other $\mathrm{re}[z_{ij}]$'s. Tayrani *et al.* [14] stated that the negative source resistance may be caused by the calibration error. Generally it is more difficult to accurately measure higher reactance values from scattering-parameter measurement, thereby the effect of calibration error on the s-to-z transformation is expected to be larger at lower frequency

TABLE II
VNA CALIBRATION ERROR

	S11		S12		S21		S22	
max.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
cal. error	0.01 dB	0.2 °	0.005 dB	0.4 °	0.005 dB	0.4 °	0.01dB	0.2 °

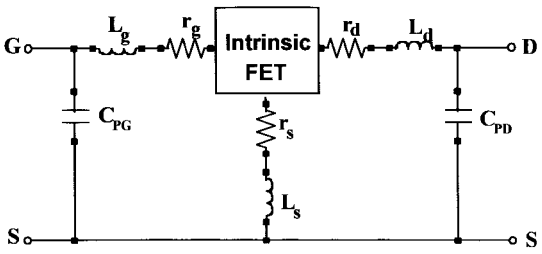


Fig. 5. A lumped-element equivalent circuit of extrinsic parameters of an FET.

range and for the pinched-off region where the capacitive part is dominant in impedance. However, as shown in Fig. 4(a), the two solid lines of $\mathrm{re}[z_{21}]$, which are minimum and maximum bounds caused by the calibration error, do not show that the negative source resistance at high-frequency range comes from the calibration error. The error bounds were calculated assuming the maximum and constant calibration errors at all the frequencies (worst-case calculation). The calibration errors in magnitude were determined from the open S_{11} and S_{22}, and thru S_{21} and S_{12}. The phase error could not be determined from the calibration. Actually, the phase errors were determined from the values of [18]. The VNA calibration error values used in the calculation are listed in Table II.

Since the prepared FET's for r_s determination are for the low-power application, the effect of pad parasitic capacitances $C_{\mathrm{PG}}, C_{\mathrm{PD}}$, as shown in Fig. 5, should be deembedded [19]. The dependence of $\mathrm{re}[z_{21}]$ on deembedded pad capacitance values at the pinched-off cold-FET condition ($V_{\mathrm{GS}} = -1$ V and $V_{\mathrm{DS}} = 0$ V) for MESFET B is shown in Fig. 4(b). The effect of deembedding on-wafer pad capacitances on $\mathrm{re}[z_{21}]$ is appreciable. $\mathrm{Re}[z_{21}]$ increases as the pad parasitic capacitance value increases. Pad capacitances were determined from the measured open-pattern scattering parameters. The values were $C_{\mathrm{PG}} \approx C_{\mathrm{PD}} \approx 25$ and 20 fF for MESFET's and HEMT's, respectively. On-wafer measurement pads are ground–signal–ground (G–S–G) types and the size of each on-wafer probing pad is 100 $\times$ 100 μm^2 for MESFET's and 80 $\times$ 80 μm^2 for HEMT's. All the center-to-center G–S spacing is 150 μm. The different pad capacitances are caused by the different pad geometry. We confirmed that the pad capacitance values are similar to those calculated from the electromagnetic (EM) simulator HP momentum.

After deembedding pad parasitics, fitting of $\mathrm{re}[z_{21}]$ to (C1b) has been performed for three types of FET's. The result of fitting is shown in Fig. 4(c). In fitting some, lower frequency data were excluded to avoid the possible error caused by the low-frequency fluctuation. The fitting is somewhat inaccurate. For example, when compared to the dc measurements, the resistances R_p's, which reflect leakage currents, are only accurate within the same factor. In fitting, it is difficult

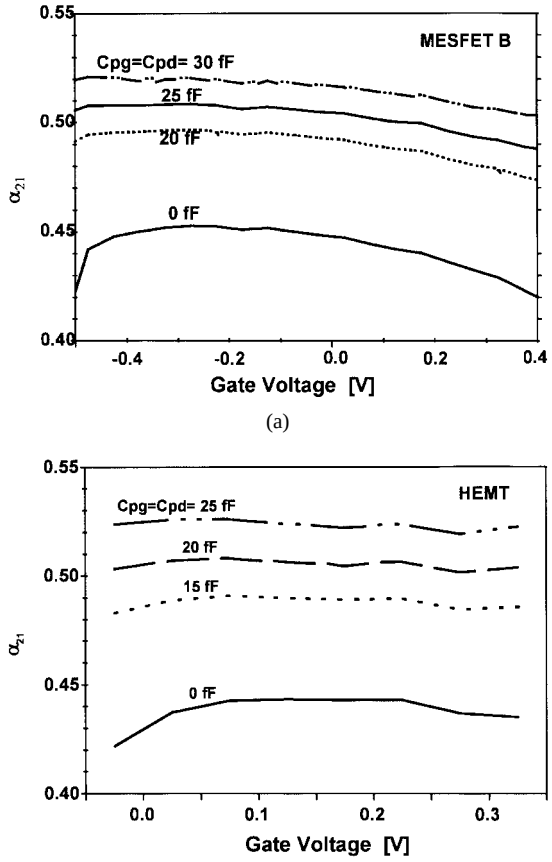


Fig. 6. Gate bias dependence of α_{21}'s for MESFET A, B, and the HEMT. Values of α_{21} goes to 0.5 after deembedding the pad parasitic capacitance $C_{\mathrm{PG}} = C_{\mathrm{PD}} = 25$ and 20 fF for the MESFET's and the HEMT, respectively. (a) MESFET B. (b) HEMT.

to determine the valid frequency range to avoid the effect of the calibration error, so the determined gate resistance is somewhat dependent on the fitting frequency range. The gate-bias dependence of α_{21} for MESFET B and HEMT is shown in Fig. 6(a) and (b), respectively. Values of α_{21} were calculated using (8). After deembedding the pad capacitances, the α_{21} values are 0.5 within $\pm 2\%$ for the selected bias ranges and for all the FET's. The sequences used for the bias-dependent r_s determination are summarized as follows:

1) if necessary, deembed pad parasitics to recalculate $\mathrm{re}[z_{ij}]$'s;
2) determine α_{21} and α_{12} from (8) and (9), respectively;
3) determine α_{11} from (7);
4) at the pinched-off cold-FET condition, determine r_g using (10);
5) determine bias-dependent r_s, r_d, and r_{ds} using (1)–(3).

In sequence 1), pad parasitics should be deembedded for FET's of the low-power application because the gate–source capacitance C_{gs} in this case is not much larger than the pad capacitances, thereby the effect of pad capacitances cannot be ignored. Pad capacitances can be determined by optimizing the measured scattering parameters of an open pattern, simulation by an EM simulator, and/or calculation from the best values, which result in the least deviation from $\alpha_{12} = \alpha_{21} = 0.5$.

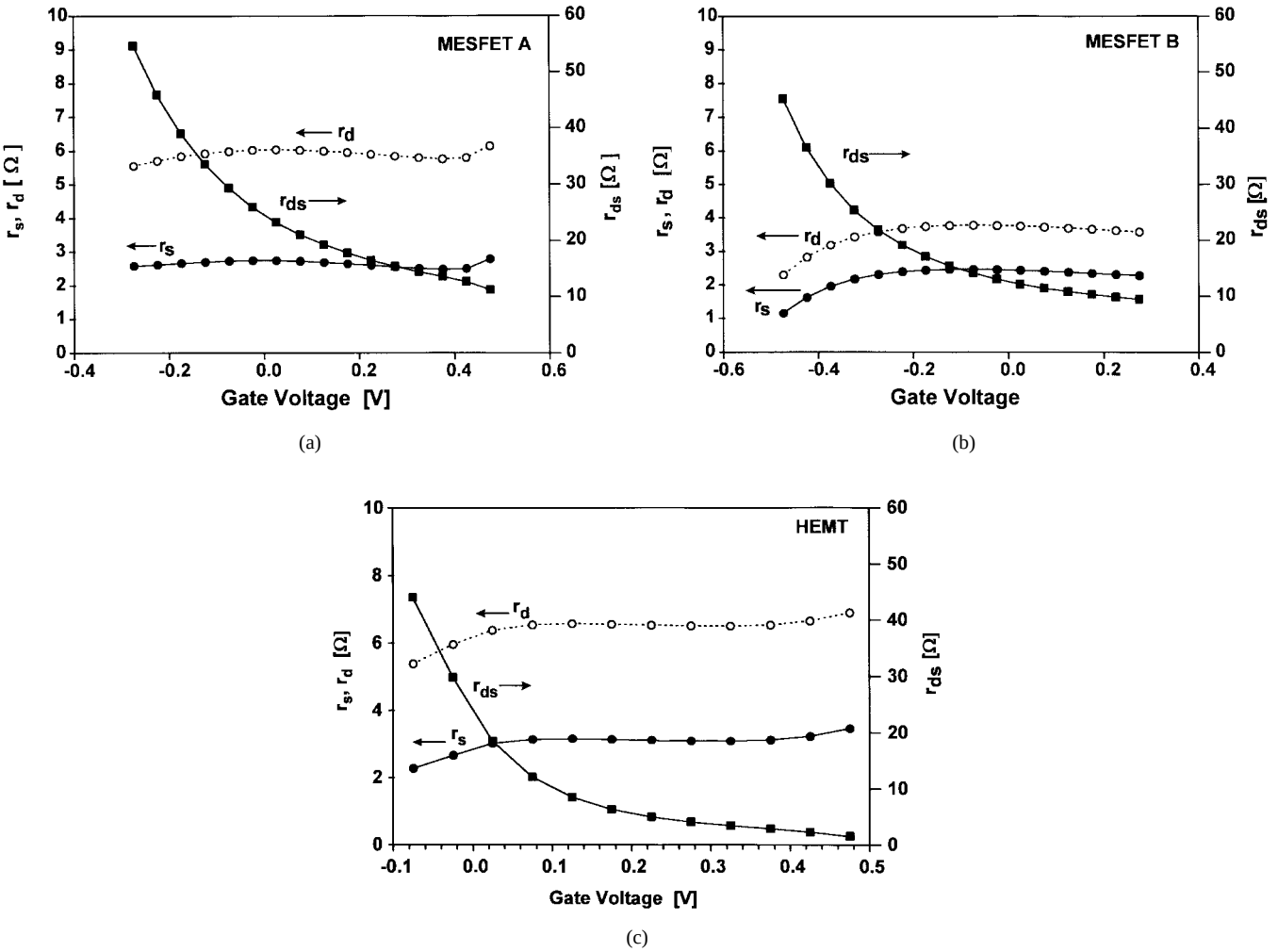


Fig. 7. Bias dependence of r_s, r_d, and $r_{\rm ds}$ at the cold-FET condition. (a) MESFET A. (b) MESFET B. (c) HEMT.

Bias-dependent r_s, r_d, and $r_{\rm ds}$ for three types of cold FET's using the above extraction procedure are shown in Fig. 7(a)–(c). The gate bias range shown was selected to avoid resistance peaks caused by the distributed resistors and capacitors. The range was also upper bounded by the condition of (6). Weak gate bias dependence of r_s and r_d is observed for all the FET's. This seems to not be consistent with the result of Sommer's [15], which showed some gate bias dependency of source resistance. Considering that Sommer's result showed an appreciable bias dependence in the negative-gate bias range, the difference may be caused by the higher pinchoff voltage of our FET's. Actually, r_s and r_d of our FET's show more gate-bias dependence at the negative gate bias region. In case of uniform doping concentration, the source and drain resistances $r_{s,d}$ can be approximated as $r_{s,d} - r^o_{s,d} \propto L_{\rm GS,GD} - c\sqrt{V_{\rm bi} - V_{\rm gs}}$. Here, $r^o_{s,d}$ is the ohmic contact resistances of source or drain, and $V_{\rm bi}$ is the built-in potential. Hence, the saturation of r_s and r_d at forward bias range is caused by the saturation of depletion region as gate bias approaches the built-in potential. The extracted parasitic resistances are summarized in Table I. As predicted in this paper, average values of α_{21} are 0.5 with errors smaller than 1% (0.499, 0.502, and 0.505 for MESFET A, MESFET B, and HEMT, respectively). The gate resistances of MESFET's are inversely proportional to gate lengths with some error of 11%, i.e., $[L_G(A)/L_G(B)]/[r_g(B)/r_g(A)] \approx 1.11$. For r_s and r_d, the resistance values are not simply proportional to the spacings $L_{\rm GS}$ and $L_{\rm GD}$ because ohmic contact resistances should also be considered. Nevertheless, the self-consistency between determined source and drain resistances supports the validity of this method.

V. Conclusions

A new method to determine bias-dependent source resistances has been introduced. The method has advantages in the fact that it needs only one assumption of laterally symmetric channel-doping profile and simple algebraic calculations. In addition, it allows one way to deembed pad parasitic capacitances. However, the valid gate bias range in the determination of parasitic resistances is bounded as discussed and the error in gate resistance determination at the pinched-off cold-FET condition may limit the accuracy of the method unless frequency range of fitting should be carefully selected. Nevertheless, seeing the accuracy and self-consistency in our results, the method described in this paper is useful in characterizing GaAs FET's.

APPENDIX A

The $ABCD$ matrix for the two-port network in Fig. 1(b) is expressed as

$$\begin{bmatrix} v_{1i} \\ i_{1i} \end{bmatrix} = \begin{bmatrix} 1+\Delta r_c \cdot \Delta y & \{(1+\Delta r_c \cdot \Delta y)^2 - 1\}/\Delta y \\ \Delta y & 1+\Delta r_c \cdot \Delta y \end{bmatrix} \cdot \begin{bmatrix} v_{2i} \\ -i_{2i} \end{bmatrix}. \quad \text{(A1)}$$

After cascading the small FET's, the relations between the two-port currents and voltages are

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \boldsymbol{M} \cdot \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \quad \text{(A2)}$$

where

$$\boldsymbol{M} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \lim_{m\to\infty} \prod_{i=1}^{m} \begin{bmatrix} 1+\Delta r_c \cdot \Delta y & ((1+\Delta r_c \cdot \Delta y)^2-1)/\Delta y \\ \Delta y & 1+\Delta r_c \cdot \Delta y \end{bmatrix}.$$

Here, m is the number of the small FET's. For the cold-FET bias condition, i.e., $V_{\rm DS} = 0$ V and FET's having a laterally symmetric channel profile, the following equation also holds:

$$\begin{bmatrix} v_2 \\ i_2 \end{bmatrix} = \boldsymbol{M} \cdot \begin{bmatrix} v_1 \\ -i_1 \end{bmatrix}. \quad \text{(A3)}$$

From (A2) and (A3), $A = D$ and $A^2 - BC = 1$ are obtained. Using $v_1 = v_{\rm gs}$, $v_2 = v_{\rm gs} - v_{\rm ds}$, $i_1 + i_2 = i_g$, and $i_2 = -i_d$, (A2) and (A3) can be reformulated to the ac current–voltage relationships among the gate–source and gate–drain ones as follows:

$$v_{\rm gs} = \frac{A}{C}\, i_g + \frac{A-1}{C}\, i_d \quad \text{(A4)}$$

$$v_{\rm ds} = \frac{A-1}{C}\, i_g + \frac{2(A-1)}{C}\, i_d. \quad \text{(A5)}$$

From (A4) and (A5), the intrinsic z-parameters are

$$\begin{aligned} z'_{11} &= A/C \\ z'_{21} &= z_{12} = (A-1)/C \\ z'_{22} &= 2(A-1)/C \end{aligned} \quad \text{(A6)}$$

where the prime represents the intrinsic part. From (A6), the following condition is obtained:

$$z'_{12} = z'_{21} = z'_{22}/2. \quad \text{(A7)}$$

Condition (A7) has been proven in [6] when channel resistance is uniform. We have proven that condition (A7) is satisfied in the more general case when the lateral channel-doping profile is symmetric.

APPENDIX B

As shown in Fig. 2, using the linear depletion approximation out of the gate, the depletion width out of the gate is

$$W(x) \approx W_o - x, \qquad \text{for} \quad 0 < x < W_o - W_s. \quad \text{(B1)}$$

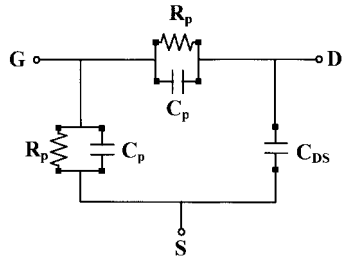


Fig. 8. A lumped-element equivalent circuit of an intrinsic part of a pinched-off cold-FET. Here, the prime represents the intrinsic part of the FET.

Assuming uniform channel resistivity per channel length ρ, the incremental resistance per unit gatewidth between x and $x+dx$ by the gate bias change is approximated as $(\Delta W/[a - W(x)]^2) \cdot \rho \cdot dx$. Thus, the change of the out-of-gate channel resistance by the gate voltage is expressed as

$$\begin{aligned} &\Delta r_{\rm ds}(\text{out-of-gate}) \\ &\quad \approx 2 \cdot \int_0^{W_o - W_s} (\Delta W/[a - W(x)]^2) \cdot \rho \cdot dx \\ &\quad = 2 \cdot \rho \cdot \Delta W \cdot \int_0^{W_o - W_s} \frac{dx}{(a - W_o + x)^2} \\ &\quad = 2\rho \cdot \frac{\Delta W}{a - W_o} \cdot \tan^{-1}\left(\frac{W_o - W_s}{a - W_o}\right). \end{aligned} \quad \text{(B2)}$$

APPENDIX C

At the pinched-off cold FET condition, the lumped-element equivalent circuit can be described, as shown in Fig. 8. From the current–voltage relations between the gate, source, and drain ports, the real part of the two-port z-parameters of common-source FET's can be expressed as follows:

$$\text{re}[z_{11}] = r_g + r_s + \frac{R_p[1 + (\tau_p + \tau_{\rm ds})^2 \cdot \omega^2]}{[1 + \tau_p^2\omega^2] \cdot [1 + (\tau_p + 2\tau_{\rm ds})^2\omega^2]} \quad \text{(C1a)}$$

$$\text{re}[z_{21}] = \text{re}[z_{12}] = r_s + \frac{R_p}{1 + (\tau_p + 2\tau_{\rm ds})^2\omega^2} \quad \text{(C1b)}$$

$$\text{re}[z_{22}] = r_s + r_d + \frac{2R_p}{1 + (\tau_p + 2\tau_{\rm ds})^2\omega^2} \quad \text{(C1c)}$$

where $\tau_p = R_p \cdot C_p$ and $\tau_{\rm ds} = R_p \cdot C_{\rm ds}$. Here, the relations $C_{\rm gs} = C_{\rm gd} = C_p$ and $R_{\rm gs} = R_{\rm dg} = R_p$ were used from the symmetry consideration. The resistance R_p comes from the leakage current. From (C1a) to (C1c), it is expected that the frequency dispersion in the real part of the z-parameters is observed when the leakage current is not negligible.

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Chung-Hwan Kim received the B.S., M.S. and Ph.D. degrees in physics from the Seoul National University, Seoul, Korea, in 1985, 1987 and 1993, respectively. His Ph.D. dissertation was on the fabrication and characterization of trapping phenomena on III–V metal-insulator-semiconductor structures.

Since 1993, he has been with the Electronics and Telecommunications Research Institute (ETRI), Taejon, Korea, as a Senior Engineering Staff Member, where he has worked on the design and testing of the GaAs-MESFET radio-frequency (RF) integrated circuits (IC's) in wireless applications, as well as the characterization and modeling of GaAs MESFET's. He is currently working on the design and testing of the CMOS RF IC's in wireless applications.

Kyung-Sik Yoon (M'80) was born in Kyunggi-do, Korea on March 7, 1949. He received the B.S. degree in electronics from the Seoul National University, Seoul, Korea, in 1971, the D.E.A degree in electronics and instrumentation from the Universite Louis Pasteur, Strasbourg, France, in 1977, and the Ph.D. degree in electrical engineering from and University of Utah, Salt Lake City, in 1988.

From 1978 to 1982, he worked as a Research Engineer at the Korea Ocean Research and Development Institute. In 1988, he joined the Department of Electronics and Information Engineering, Korea University, Choong-Nam, Korea, where he is currently a Professor. His current research interests are in compound semiconductor device modeling, microwave and millimeter-wave device characterization and model parameter extraction, their accurate measurement techniques, and microwave circuit design.

Jeon-Wook Yang received the B.S degree in electronic engineering from Kwangwoon University, Taegu, Korea, in 1981, and the M.S. and Ph.D. degrees in electronic engineering from Yonsei University, Seoul, Korea, in 1983 and 1994, respectively.

After joined the Electronics and Telecommunications Research Institute (ETRI), Taejon, Korea, in 1985, he had been involved in the development of semiconductor devices and processes using compound semiconductors. Since 1989, he has been working on the development of GaAs MESFET and HEMT and their integrated circuits. He is currently a Principal Research Staff Member in the Department of Compound Semiconductors, Electronics and Telecommunication Research Institute, Taejon, Korea.

Jin-Hee Lee received the B.S. degree in physics, and the M.S. and Ph.D. degrees from Youngnam University, Taejon, Korea, in 1980, 1982, and 1987, respectively.

In 1984, he joined the Electronics and Telecommunications Research Institute (ETRI), Taejon, Korea. From 1984 to 1992, he was involved in developing the fine-line lithography, multilevel interconnection, and fabrication process of GaAs MESFET's. In 1993, he was dispatched for one year to University of Tokyo, Tokyo, Japan, to perform international research. Since returning from Japan, he has been involved in development of high-speed devices and their integrated circuit. He is currently a Principal Research Staff Member in the Department of Compound Semiconductors. His current research interests include fabrication and characterization of the low-noise GaAs and InP-based HEMT devices for millimeter-wave monolithic microwave integrated circuit (MMIC) applications, nanometer devices, and optical devices.

Chul-Soon Park (M'97) received the B.S. degree in metallurgical engineering from the Seoul National University, Seoul, Korea, in 1980, and the M.S. and Ph.D. degrees in materials science from the Korea Advanced Institute of Science and Technology, **City,** Korea, in 1982 and 1985, respectively.

In 1985, he joined the Electronics and Telecommunications Research Institute (ETRI), Taejon, Korea, where he had been involved in the development of semiconductor devices and processes. From 1987 to 1989, he was with AT&T Bell Laboratories, Murray Hill, NJ, where he studied the initial growth of group IV semiconductors. Since 1989, he has been involved in the development of compound semiconductor devices and their application to microwave and high-speed integrated circuits. He is currently the Head of the Compound Semiconductor Device Section and a Principal Research Staff Member at ETRI.

Jae-Jin Lee received the B.S. degree in physics from the Kongju National Teacher's College of Chung-nam, Chung-nam, Korea, in 1975, and the M.S. and Ph.D. degrees in solid-state physics from the Dongkuk Univertsity of Seoul, Seoul, Korea, in 1980 and 1986, respectively.

In 1987, he joined the Compound Semiconductor Department, Electronics and Telecommunications Research Institute (ETRI), Taejon, Korea. From 1987 to 1990, he worked on molecular beam epitaxy (MBE) growth for low-noise HEMT devices applications. From 1991 to 1992, he was a Visiting Scientist at the Massachusetts Institute of Technology (MIT), Cambridge, where he worked on heterojunction bipolar transistors (HBT's) for high-power high-speed applications. Since 1990, he has been involved in the development of GaAs/AlGaAs and InGaAs/InAlAs/InP epitaxial layer for power MESFET's and low-noise amplifier's. He is currently Head of the Microwave Circuit Section and is a Principal Member of the technical staff at ETRI, where he is responsible for the design and fabrication of MMIC's of wireless communications.

Kwang-Eui Pyun (M'97) received the Ph.D. degree in electronic engineering from Yonsei University, Seoul, Korea in 1990.

From 1980 to mid-1981, he was a Research Assistant in the Electronic Engineering Department, Yonsei University. From mid-1981 to 1984, he was a Full Instructor in the Electronic Engineering Department, Korea Naval Academy. In mid-1984, he joined the Electronics and Telecommunications Research Institute (ETRI), Taejon, Korea, to perform semiconductor field research. From 1984 to 1992, he was a Senior Technical Staff Member in the Compound Semiconductor Department. In 1993, he was dispatched for one year to the Electric and Electronic Department, University of Tokyo, Tokyo, Japan, to perform international research activities. Upon returning from Japan, he was in charge of processing laboratories, including silicon and compound semiconductor fields for one year. Since 1995, he has been in charge of the Compound Semiconductor Department, ETRI. His main areas of interest are compound-based processing fields, including GaAs and InP, and especially high-frequency and opto-electronic devices.